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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):

Philip J. Kuekes et al.

Confirmation No.: 5021

**Application No.:** 10/659,892

Examiner: Guy J. Lamarra

Filing Date:

09/10/2003

**Group Art Unit: 2133** 

Title:

DEFECT-TOLERANT AND FAULT-TOLERANT CIRCUIT INTERCONNECTIONS

**Commissioner for Patents** PO Box 1450 Alexandria, VA 22313-1450

## PETITION FOR EXTENSION OF TIME

Sir:

In an Office Action ma	ailed on04/21/2006	, on the above-identified U.S	. Patent
application, a shortened s	tatutory period of3	months was set for response.	In accordance
with 37 C.F.R. 1.136(a), applicant(s) hereby request(s) a:			
<b>(X</b> )	one month		
( )	two months		
( )	three months		
( )	four months		

time extension so that the period for response to the Office Action expires on \_08/21/2006 Authorization to charge the fee required by 37 CFR 1.17 to Deposit Account 08-2025 appears in the enclosed transmittal letter. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as :

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Date of Deposit: Aug. 21, 2006

Typed Name: Joanne Bourguignon

Respectfully submitted,

Philip J. Kuekes et al.

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Date: Aug. 21, 2006

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08/28/2006 DEMMANU1 00000053 082025 10659892 120.00

Rev 12/04 (Ext Time)

Signature: